REMARKS

Applicant respectfully requests reconsideration and allowance of the subject application. Claims 1-3, 6-15, and 18-22 are pending. Claims 1, 3, 6, 8, 9, 10, 11, 12, 19, 21, and 22 have been amended. Claims 2 and 20 have been canceled.

The present Office Action has been made final. With respect to this finality, the Applicant respectfully traverses. The Examiner, in paragraph 8 of the Office Action, has indicated that the Applicant's previous amendment necessitated the new grounds of rejection. The amendments made in the prior response, however, merely combined the limitations previously contained in multiple claims into a single claim (i.e, the limitations in claims 1, 4, and 5 were combined into amended claim 1 and the limitations of claims 13, 16, and 17 were combined into amended claim 13). All of the elements of the amended claims were present in the claims as originally filed and were examined by the Examiner in the initial examination. Thus, the new grounds of rejections were not necessitated by Applicant's previous amendment, and, thus, the present Office Action should be non-final. Accordingly, the Examiner is respectfully requested to reconsider and withdraw the finality of the Office Action.

ALLOWABLE SUBJECT MATTER

Claims 3, 6-7, 14-15, 18, and 21-22 are indicated as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim. Applicant appreciates the indication of allowability.

35 U.S.C. §102 Claim Rejections

The Examiner has rejected claim 1 as being anticipated by U.S. Patent No. 6,326,842 to Kuroda (hereinafter "Kuroda"). Claim 1 has been amended to incorporate the elements previously found in claim 2, thus rendering moot the rejection under 35 U.S.C. §102.

35 U.S.C. §103 Claim Rejections

The Examiner has rejected claim 2, 8-9, 11-13, and 19-20 as being unpatentable over Kuroda in view of U.S. Patent Application No. US2002/0021169 A1 to King, et al. (hereinafter "King"). Applicant respectfully traverses these rejections.

The Claimed Invention

The claimed invention is directed to an apparatus and method for effectively amplifying electrical signals. As shown in Fig. 1, a second stage power amplifier is connected to an output of a first stage power amplifier (see Fig.1 and Specification, page 4, lines 10-19). The first and second stage amplifiers are designed to operate together to efficiently deliver output power with at least two different output power levels. Each stage amplifier can be configured in at least two states. A state determination circuit selectively configures the two stage amplifiers based on criteria such as the output power level. An single output impedance matching circuit is used to allow for different impedance levels for a single device that operates at more than one output level.

Kuroda

Kuroda teaches a variable gain amplifier that provides for various levels of gain while at the same time minimizing increases in noise. The amplifier taught in Kuroda has a first

amplifying circuit, a second amplifying circuit, and a third amplifying circuit for creating various gain levels. Kuroda does not disclose any impedance matching techniques for matching the amplifier output with a particular load.

King

King teaches an amplifier for providing efficient power amplification at more than one output level. King uses two separate power devices. One power device is designed for efficiency at a first output level and is used exclusively to deliver power for a first power output range and the other power device is designed for efficiency at a second output power level and is used exclusively to deliver power for a second power output range. King teaches the use of a pair of impedance matching circuits, with the output of the amplifier directed to one of the two impedance matching circuits depending upon the output state of the amplifier.

The Examiner has not set forth a prima facie case of obviousness

As set forth in the MPEP M.P.E.P. §2143.03:

> To establish a *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Claim 1

Claim 1, as amended, recites the following:

1. An amplifier comprising:
a first stage having at least two power states comprising a first power device and a second power device connected in parallel with said first power device, said first stage having an input for receiving a data signal, a control port, and an output;
a second stage having at least two power states comprising a third power device and a fourth power device connected in parallel with said third power device, said third power device and said fourth power device each having an output, said second stage having an input coupled to the output of said first stage, a control port, and ~~an~~ a second stage output

comprising a combination of said outputs of said third power device and said fourth power device; and

a state determination circuit coupled to the control port of said first stage for selectively configuring said first stage in one of the at least two power states and further coupled to the control port of said second stage for selectively configuring said second stage in one of the at least two power states.; and

an output impedance matching circuit having at least two impedance matching states, said output impedance matching circuit having an input coupled to the second stage output, a control port, and an output for coupling to a load, said state determination circuit further for selectively configuring said output impedance matching circuit in one of the at least two impedance matching states.

Neither Kuroda nor King teach or suggest using an output impedance matching circuit coupled to the output of the second stage of the amplifier, with the impedance matching circuit having at least two impedance matching states. Kuroda fails to teach any impedance matching function whatsoever. The addition of King fails to disclose the impedance matching circuit as claimed in claim 1.

The output impedance matching circuit shown in King uses a dual-path power amplifier having two separate matching networks, each having a single impedance state, with each network *coupled to the output of each individual power device*. A switch is used to allow for the output of each impedance network (402, 410 of Fig. 4) contained in the amplifier taught in King to be combined into a single output (408). "The combining network device (400) includes first and second matching network devices 402 and 416, and a switch 410, that together allow first and second power devices, the outputs of which are shown at 112 and 122, to share a common output port at 408." Paragraph 40, lines 3-8 of King. This combination combines the matched outputs of individual power devices. It does not provide for multi-state impedance matching of an output of a second stage that comprises a combined output of the individual power devices contained in the second state.

The present invention, as claimed in claim 1, uses a single output impedance matching circuit that has two different impedance states. This allows for two different impedance levels to be applied to the second stage output of the amplifier. The output of the second stage of the amplifier of the present invention (144 of Fig. 1, representing the combined outputs of device 136 and device 138) is coupled to the output impedance matching circuit. The level of impedance in the output impedance matching circuit is controlled by the state determination circuit, as described on page 13, lines 1-10 of the specification.

The use of an impedance matching circuit containing two states coupled to the output of the second stage (which comprises the combined output of the power devices in the second stage) is clearly set forth in amended claim 1, which recites *an output impedance matching circuit having at least two impedance matching states, said output impedance matching circuit having an input coupled to the output of said second stage*.

Because neither Kuroda nor King teach or suggest one output impedance matching circuit having at least two impedance matching states, with the input of the impedance matching output coupled to the output of the second stage of the amplifier, the rejection under 35 U.S.C. §103 should be withdrawn.

Claims 8-12

Claims 8-12 depend from claim 1, and thus are allowable for the same reason as claim 1.

Claim 13

Claim 13, as currently amended, also contains the element *"an output impedance matching circuit having at least two impedance matching states, said output circuit having an input coupled to the output of said second stage."* As discussed above, this element is not taught or suggested in either Kuroda or King. Thus, claim 13 is allowable for the same reasons as set forth above.

Claim 19

Claim 19, as currently amended, recites in part the following:

> *configuring an output matching circuit in one of at least two impedance states based on said determined level, said output matching circuit matching the impedance of said second stage amplifier and the impedance of the load.*

As discussed with respect to claim 1 and claim 13, the cited art does not teach an output matching circuit that has at least two impedance states, with the output circuit matching the impedance of the second stage amplifier and of the load. As discussed above, the impedance matching circuits of the cited art are configured to match the output of a particular power device within an amplifier stage, not to match the impedance of the second stage of the amplifier. Thus, claim 19 is allowable for the same reasons as set forth above.

CONCLUSION

Claims 1, 3, 6, 7-15, 18-19, and 21-22 are currently in condition for allowance. Applicant respectfully requests reconsideration and issuance of the subject application. If any issues remain that preclude issuance of this application, the Examiner is urged to contact the undersigned attorney.

Respectfully Submitted,

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